AMENDMENTS TO THE SPECIFICATION

Please amend paragraphs [0047], [0059] and [0079] as follows:

[0047] As used herein, a first order aggressor net is an aggressor net that has a significant crosstalk influence on a given victim net. A *second* order aggressor is an aggressor net that has significant influence upon a transition waveform (or slew rate) of ~~on~~ a first order aggressor of the given victim net. It is possible that an aggressor net may serve as both a first order aggressor and a second order aggressor relative to a given victim net. The consideration of second order aggressor effects is a novel feature of the present invention that contributes to more accurate delay change analysis.

[0059] The pre-computed fast transitions on aggressor nets of the design are used during the delay change computation on each victim net, which is described in following sections below.

Piece-Wise ~~piece-Wise~~-Linear Approximation of Pre-Computed Aggressor Waveforms

[0079] The ViVo model of **Figure 6A** is employed as the nonlinear current model 626 in the embodiment of **Figure 6A**. ViVo models current response of the last CCC, such as component 608 of **Figure 6A**, of a driver 606 to voltages on input and output. The ViVo model is pre-characterized and stored in a cell library per each transition type (rise/fall) and per each input-output arc of each interface CCC of the cell, that is a CCC connected to either input or output pin of the cell CCC. ViVo models current drawn by the output pin of the CCC for various voltage values on the input and output pins. This current model is part of an embodiment of the invention that allows high accuracy of analysis due to the fact that a current drawn by a gate during switching can be well represented by a voltage-controlled current source, which is a function of instantaneous voltages on the input and output: $I_d = I(V_i, V_o)$. It is implemented as a two dimensional (2-D) current table, discussed below, describing the nonlinear (voltage-controlled) current source. In addition to the 2-D current table shown in **Figure 6B**, the ViVo CM also includes two capacitors modeling,

respectively, the Miller C_M and ground C_g capacitance of the output pin of the output of the CCC, shown in **Figure 6A.** ~~[need to update the figure]~~